WHAT IS CLAIMED IS:

1. A method for designing a circuit comprising a plurality of conductors, the method comprising:

selecting a first operating point corresponding to a first circuit application;

selecting a second operating point corresponding to a second circuit application;

determining a performance difference between circuit operation at the first and second circuit operating points;

using the performance difference to compute a factor;

applying the factor to resistance values of the conductors, thereby producing modified conductor resistance values; and

performing a timing analysis of the circuit using the modified conductor resistance values.

2. The method as recited in claim 1, wherein a result of the timing analysis indicates whether the circuit will operate correctly in the presence of one or more timing constraints.

3. The method as recited in claim 2, wherein in the event the result of the timing analysis indicates the circuit will operate correctly in the presence of the one or more timing constraints, the circuit will also likely meet performance requirements of the second circuit application.

4. The method as recited in claim 1, wherein the circuit is a functional block of a system-on-a-chip (SOC).

5. The method as recited in claim 1, wherein the conductors are interconnects.

6. The method as recited in claim 1, wherein the first and second circuit operating points exist in an environment space defined by a plurality of variable operating parameters.

7. The method as recited in claim 6, wherein the environment space is a 3-dimensional space having a process speed dimension, a power supply voltage dimension, and a circuit temperature dimension.

8. The method as recited in claim 7, wherein the selecting the first operating point comprises:

selecting a circuit temperature, thereby defining a circuit temperature plane in the 3-dimensional environment space; and

selecting a first operating point corresponding to a first circuit application within an environment window existing in the circuit temperature plane.

9. The method as recited in claim 8, wherein the first operating point is located at or near a center of the environment window.

10. The method as recited in claim 8, wherein the selecting the second operating point comprises:

selecting a second operating point corresponding to a second circuit application within the environment window.

11. The method as recited in claim 10, wherein the second operating point is located at or near an outer edge of the environment window.

12. The method as recited in claim 1, wherein the determining the performance difference comprises:

computing a performance difference factor as a ratio of a performance of the circuit at the second operating point to the performance of the circuit at the first operating point.

13. The method as recited in claim 12, wherein the using the performance difference to compute the factor comprises:

determining a factor by selecting a scaling value and multiplying the performance difference factor by the scaling value.

14. A circuit designed using the method of claim 1.

15. A computer program product for designing a circuit comprising a plurality of conductors, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer program code for applying a factor to resistance values of the conductors, thereby producing modified conductor resistance values; and

computer program code for performing a timing analysis of the circuit using the modified conductor resistance values.

16. An apparatus for designing a circuit comprising a plurality of conductors, the apparatus comprising:

means for applying a factor to resistance values of the conductors, thereby producing modified conductor resistance values; and

means for performing a timing analysis of the circuit using the modified conductor resistance values.

17. A timing analysis system, comprising:

a memory system, comprising:

software including instructions for applying a factor to resistance values of the conductors, thereby producing modified conductor resistance values;

a timing analysis tool including instructions for performing a timing analysis of the circuit using the modified conductor resistance values; and

a central processing unit coupled to the memory system and configurable to fetch instructions from the memory and to execute the instructions.